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Examiner: Do, Chat C

Group Art Unit: 2193

Total No. Pages: 24



Signature

Lawrence M. Cho

Typed or printed name of person signing Certificate

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Registration Number, if applicable

Telephone Number

Re: Serial No. 10/829,559

Attorney Docket No. ALT.P030 (A01252)

Filed: April 22, 2004

In re Application of Asher Hazanchuk et al.

Title: Method and Apparatus for Implementing a Multiplier Utilizing Digital Signal Processor Block Memory Extension

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S/N 10/829,559

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Asher Hazanchuk	Examiner:	Do, Chat C
Serial No.:	10/829,559	Group Art Unit:	2193
Filed:	April 22, 2004	Docket No.:	ALT.P030 (A01252)
Title:	Method and Apparatus for Implementing a Multiplier Utilizing Digital Signal Processor Block Memory Extension		

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RESPONSE UNDER 37 C.F.R. 1.116
EXPEDITED PROCEDURE – EXAMINING GROUP 2193

Dear Sir,

In response to the Office Action mailed April 1, 2008, Applicants respectfully request the Examiner to consider the following remarks.

Serial No. 10/829,559

1

ALT.P030 (A01252)